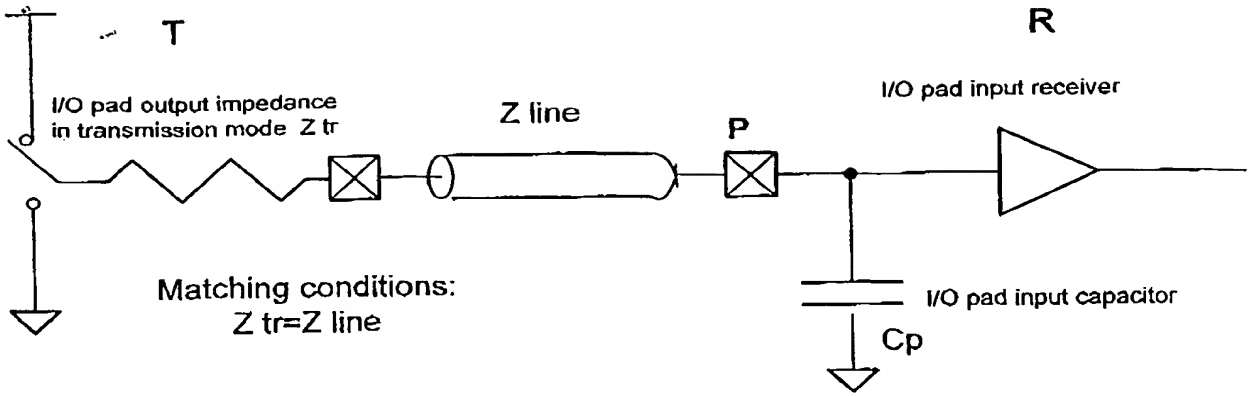


Fig1A. Serial termination

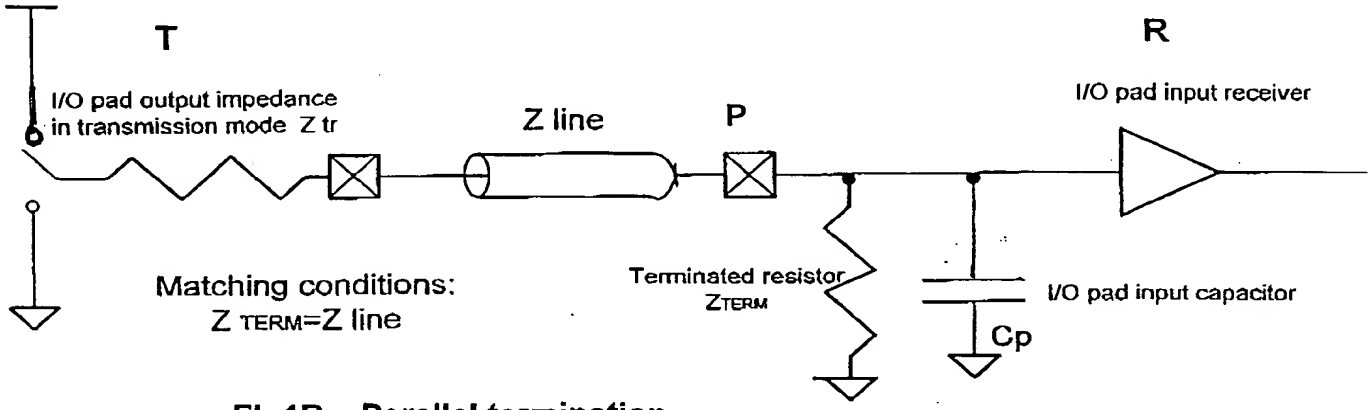


Fig1B. Parallel termination

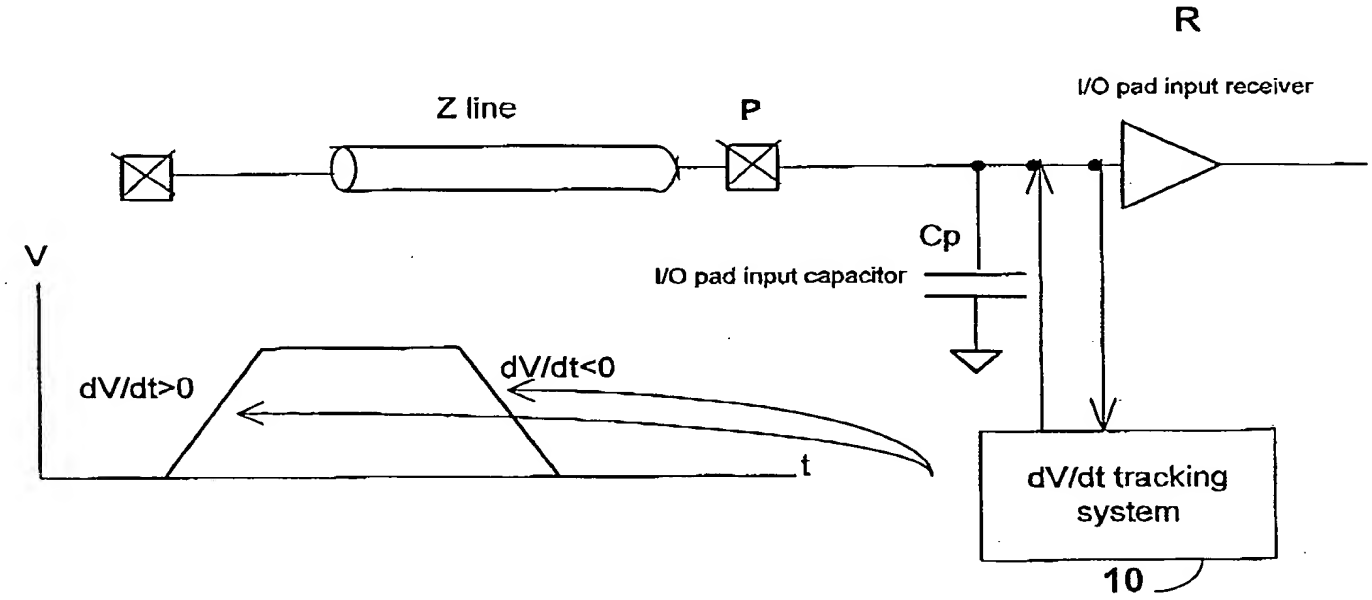


Fig2A. dV/dt tracking system

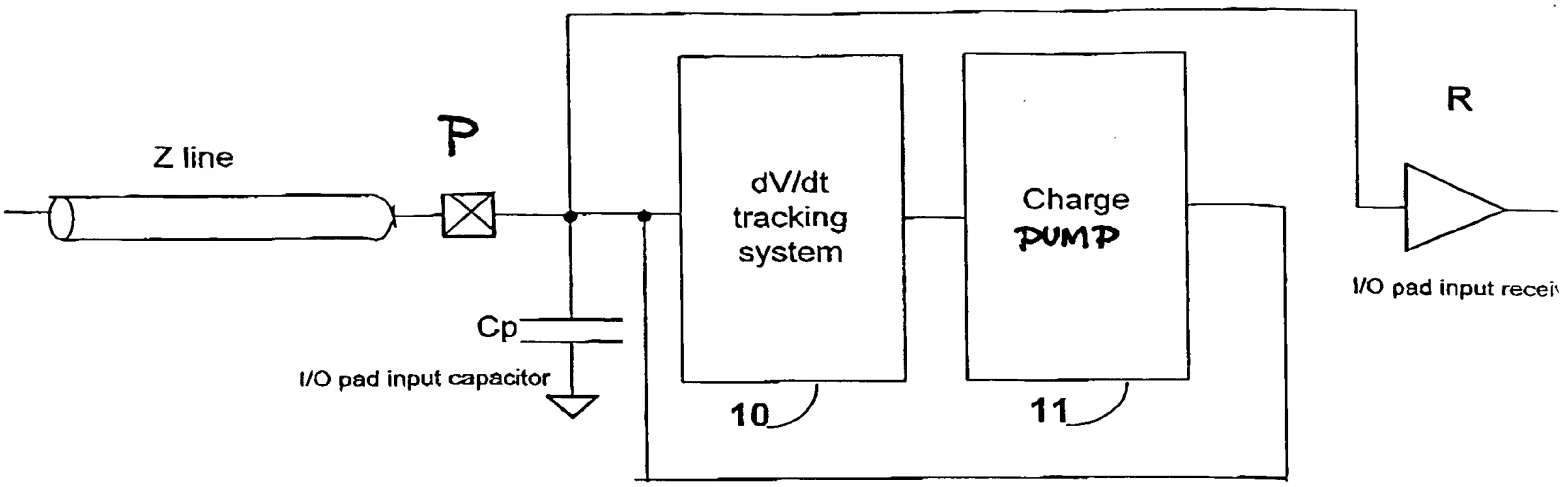


Fig. 2β dV/dt tracking system with charge pump

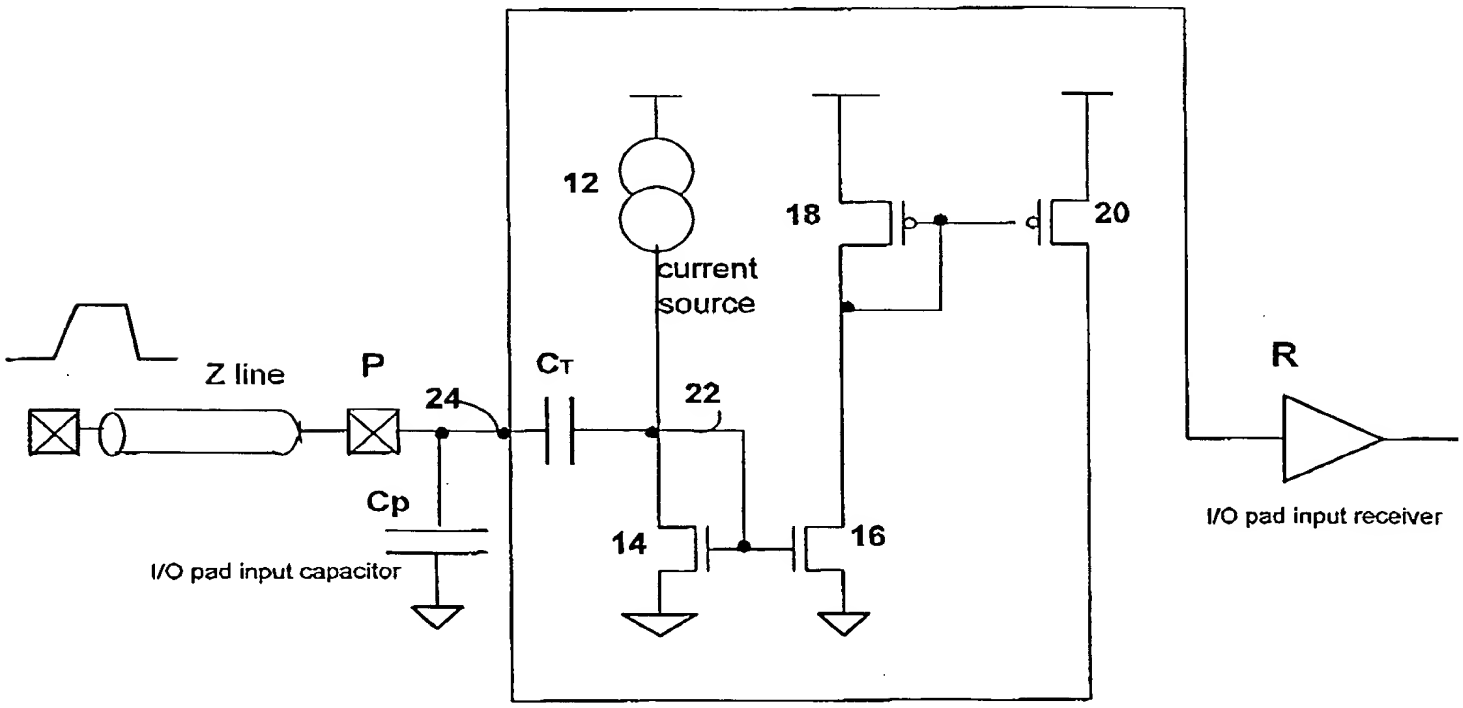
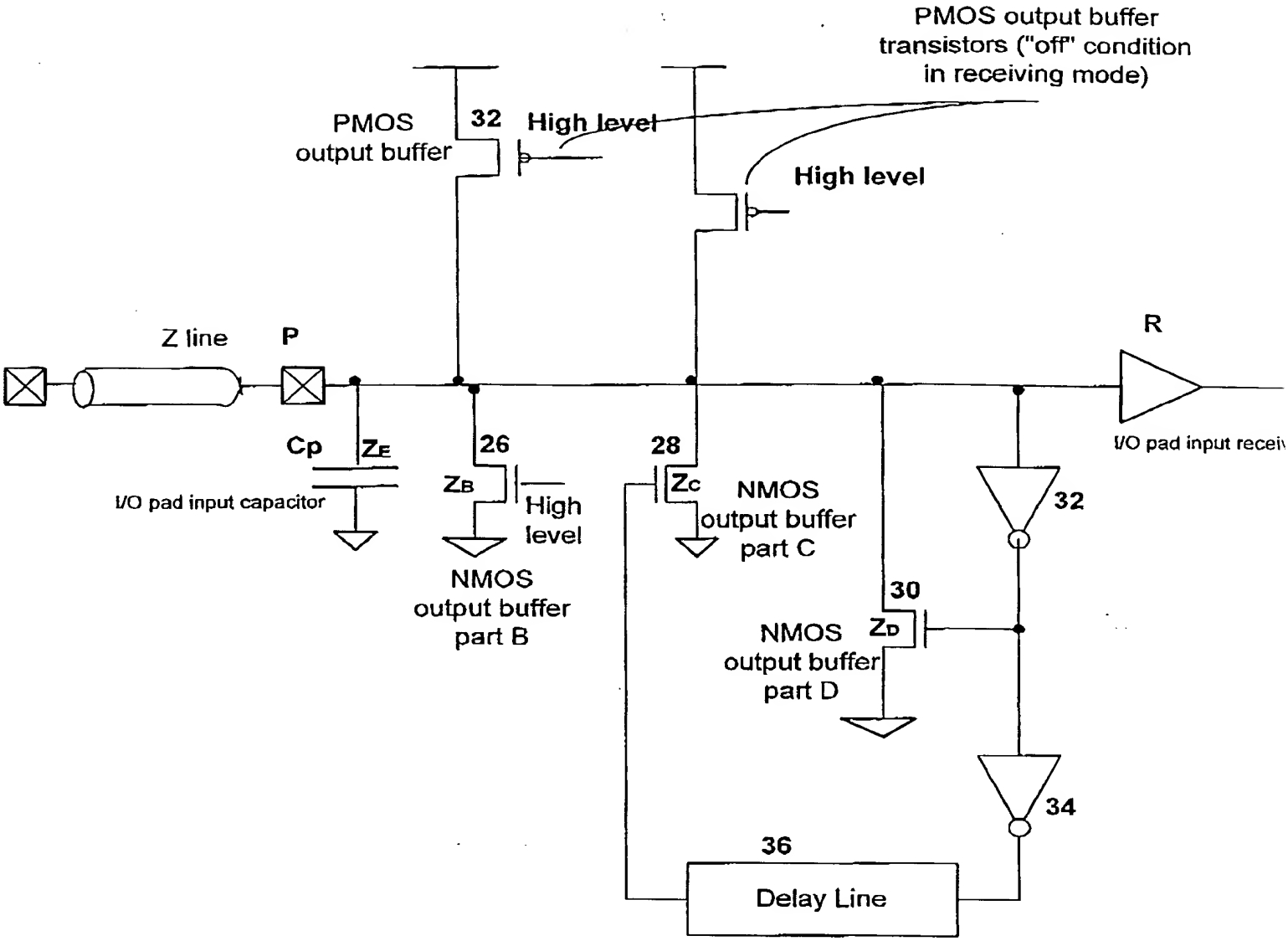


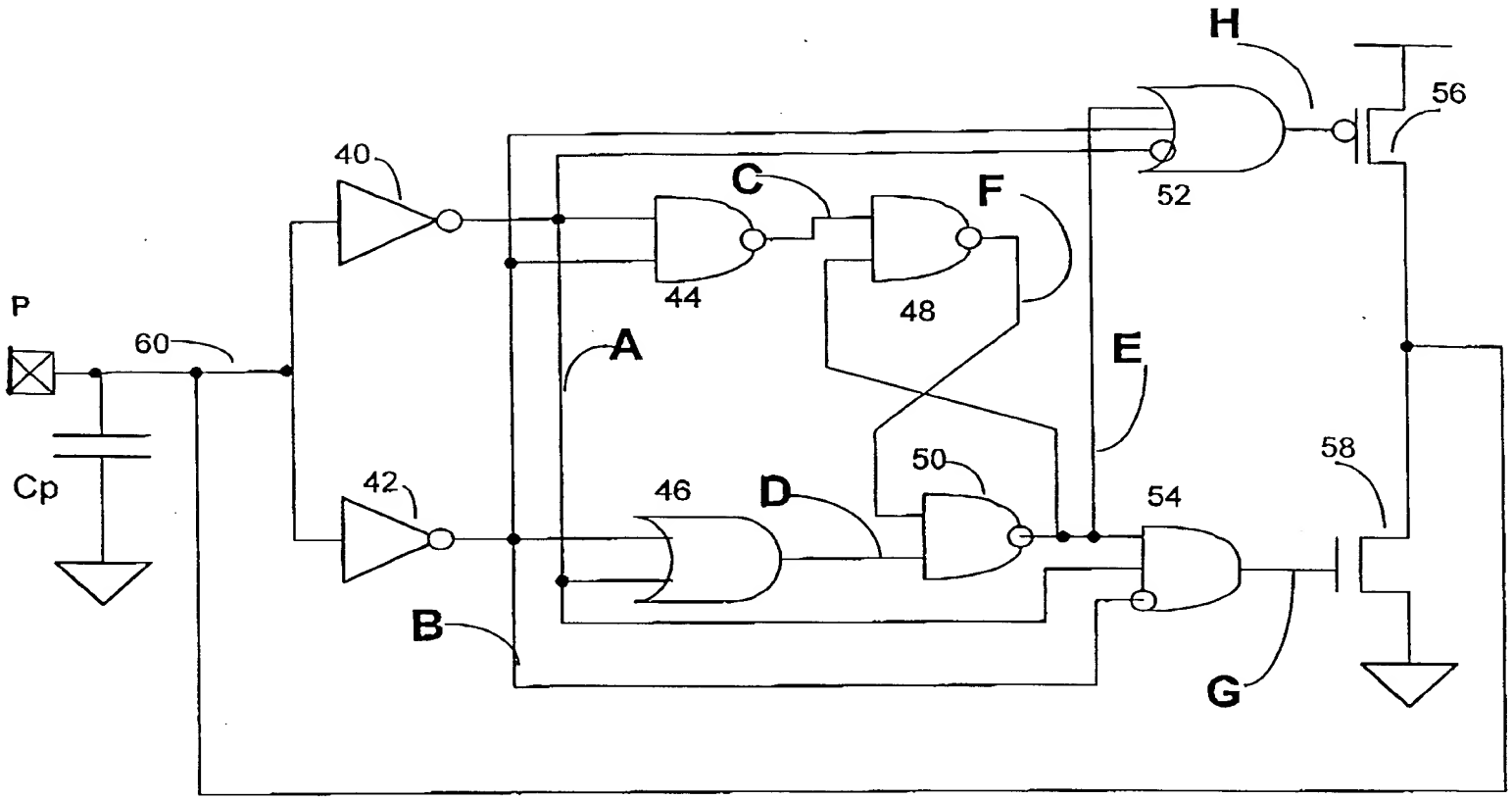
Fig. 2C. dV/dt tracking system with charge pump (more detailed)



$$Zinput = Z_B \,||\, [Z_C(or Z_D, or Z_E)]$$

if $|Z_C| = |Z_D| = |Z_E|$, then an input signal can not change Zinput

FIg. 2D NMOS output buffer parallel termination



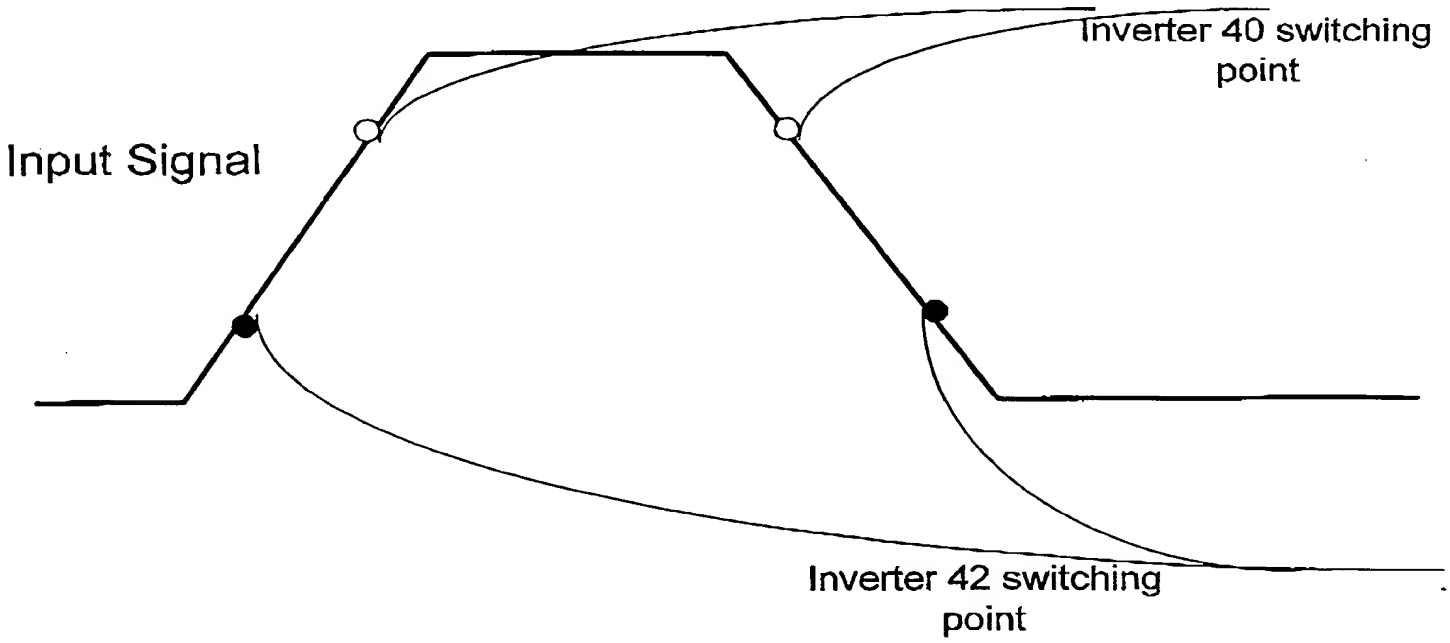


Fig. 3. An input parasitic capacitor charge/discharge circuit

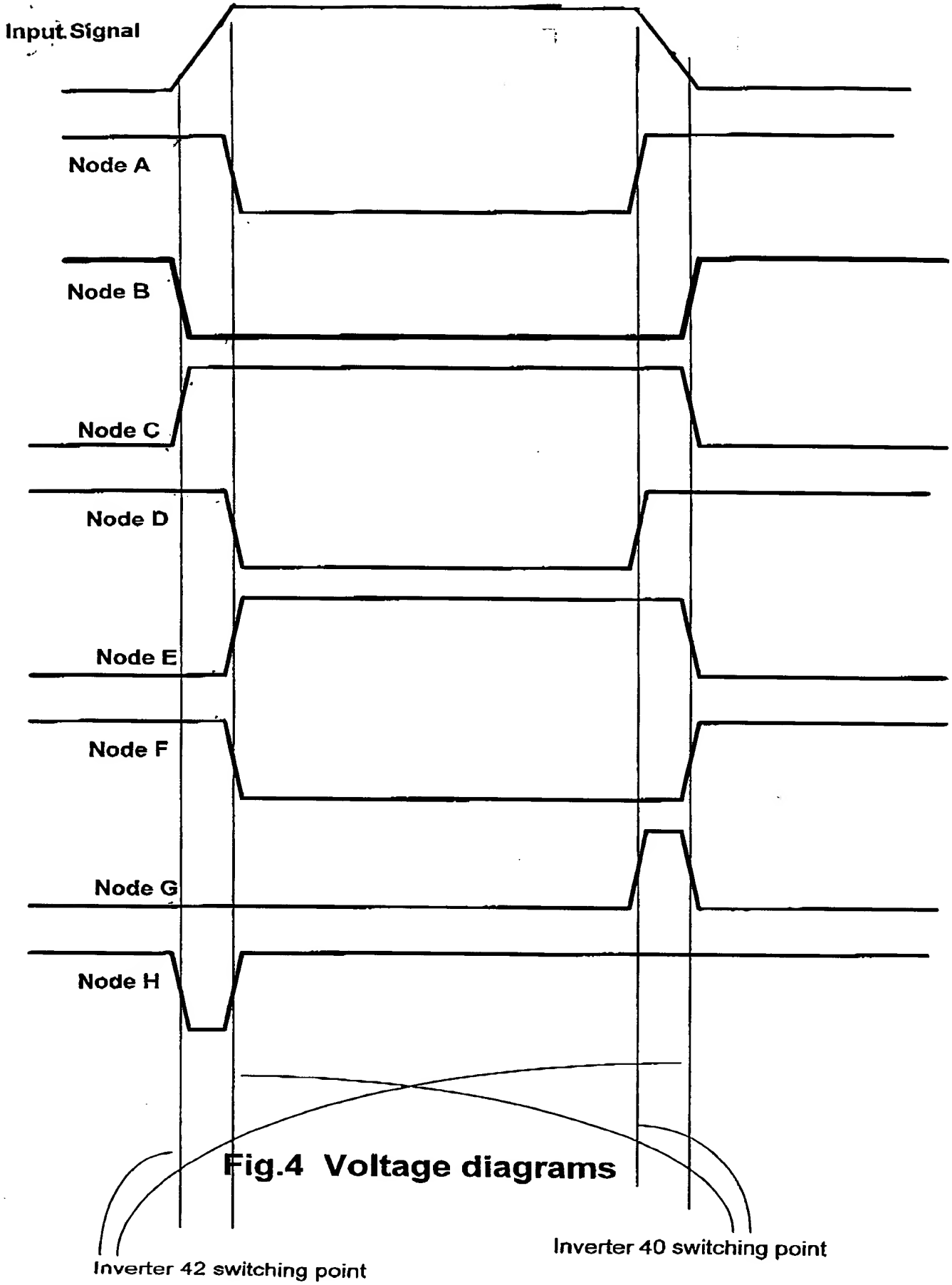


Fig.4 Voltage diagrams